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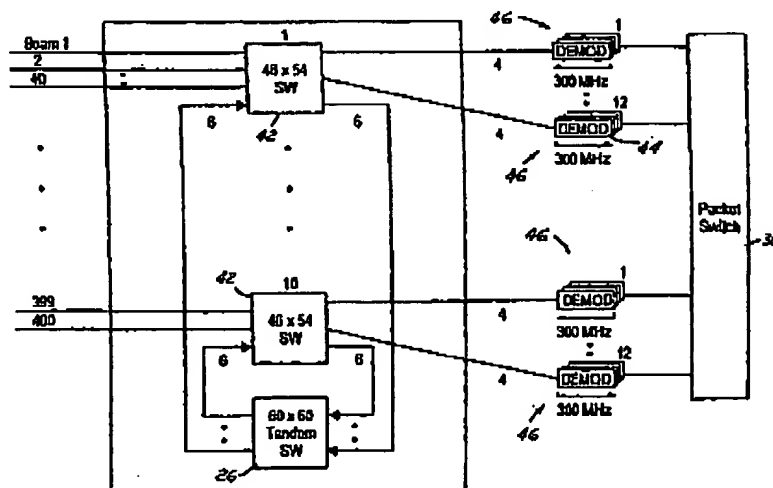
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(54) A scalable switch matrix and demodulator bank architecture for a satellite uplink receiver

(57) A scalable switch matrix and demodulator bank architecture for satellite payload processor wherein the demodulators (44; 14) are connected to the output ports of the switches (42; 24) as the data load on the uplink beams varies. The switch matrix includes a first switch layer (40; 10) for receiving the uplink transmission beams and a plurality of demodulators (44; 14) connected to the output parts of the first switch layer (40; 10).

The number of demodulators (44) is limited by the number of active uplink sub-bands which is generally less than the number of sub-bands per beam times the number of transmission beams. Thus, only a relatively few number of demodulators (44) are distributed among the uplink transmission beams as required. This results in a readily scaleable architecture having higher demodulation utilization rates than dedicated demodulation architectures.



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## EUROPEAN SEARCH REPORT

Application Number  
EP 00 11 5038

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (nl,Cl.7)
X	US 5 790 529 A (HABER WILLIAM JOE) 4 August 1998 (1998-08-04)	1-3,5-8, 10	H04B7/185
A	* column 1, line 35 - line 40 * * column 1, line 54 - line 62 * * column 2, line 31 - line 35 * * column 3, line 2 - line 6 * * column 3, line 25 - line 33 * * column 3, line 53 - line 62 * * column 4, line 27 - line 38 * * column 4, line 51 - line 67 * * column 5, line 62 - column 6, line 27 * * column 6, line 50 - line 53 * * column 6, line 59 - line 63 *	4,9	
A	EP 0 854 590 A (COM DEV LTD) 22 July 1998 (1998-07-22) * column 4, line 31 - line 52 * * column 5, line 49 - column 8, line 15 * * column 9, line 7 - line 58 *	1-10	
			TECHNICAL FIELDS SEARCHED (nl,Cl.7)
			H04B
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>12 August 2003</b>	Examiner <b>Sorrentino, A</b>
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document		T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document	

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ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.

EP 00 11 5038

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

12-08-2003

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5790529	A	04-08-1998	DE 19731475 A1	05-02-1998
			FR 2752656 A1	27-02-1998
			GB 2315959 A ,B	11-02-1998
			IT RM970449 A1	21-01-1999
EP 0854590	A	22-07-1998	US 5956620 A	21-09-1999
			EP 0854590 A2	22-07-1998
			NO 973760 A	20-07-1998
			US 6408164 B1	18-06-2002

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

## ONBOARD PROCESSOR FOR MILLIMETER-WAVE PERSONAL SATELLITE COMMUNICATIONS SYSTEM

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### ABSTRACT

This paper introduces the design of a personal satellite communications system that should be available in early decade of the next century.

In this system, an onboard processor plays an important role and its performance directly determines such features as the switch capacity and connection processing speed. In this paper, functional and performance requirements of the onboard processor are described with several effective architectural methods required in realizing such a performance. A trial model in which these features will be evaluated, is also described.

### 1. INTRODUCTION

Personalization is the most important trend in the design of communications systems, and this has led to proposals for a personal satellite communications system using millimeter-wave frequency bands [1][2].

The combination of millimeter-wave bands and an onboard processor with baseband switching promises to meet the requirements of personal communications systems: portability, low cost, and large capacity. Figure 1 shows the schematic configuration of a transponder for millimeter-wave satellite communications. The Space Communications Research Corporation (SCR) has developed millimeter-wave components such as a 50 GHz LNA and a 40 GHz TWTA, and an onboard processor with baseband switching. These technologies promise to enhance the performance of the previously proposed system. They should contribute to the key concepts of personalization, portability and lowcost, by making earth stations smaller and simpler, and by greatly increasing their user capacity.

Since the onboard processor will play an important role in this system, we have paid special attention to its design and development. A trial model which uses digital signal processing techniques and a new switching architecture has been constructed and evaluated.

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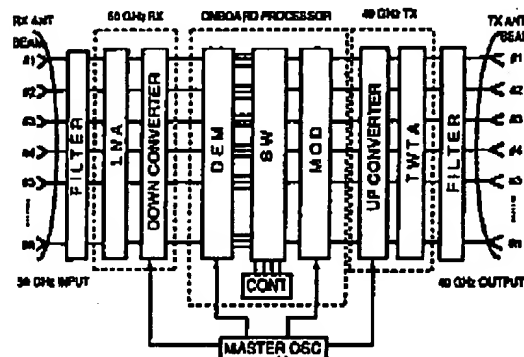


Fig. 1 Schematic configuration of transponder for millimeter-wave personal satellite communications system

### 2. MAIN FEATURES

In this system, user access the satellite using portable hand-held stations, allowing communications to be carried out at any time, anywhere.

Additionally, the data rate is 64 kb/s per channel, offering a broad range of convenient and low-cost services, including video, data transmission like ISDN, for mobile use and in rural areas. In this way, the future personal satellite communications system promises to be a powerful competitor of terrestrial communications systems.

Table 1 shows the design targets for future personal satellite communications system.

#### 2.1 Multiplex Scheme

A suitable multiplex scheme for the uplink and downlink can be chosen by having onboard baseband switching. By using SCPC-FDMA for the uplink and TDM scheme for the downlink, the power amplifiers are used effectively up to their saturation level in both links. Additionally, since an SCPC-FDMA uplink does not require a very high EIRP and exact transmission timing adjustment, as do uplinks in TDMA systems, portable earth stations become feasible.

Table 1 Parameters of future personal satellite communications system

Frequency (up / down)	50 / 40 GHz
Multiplex scheme (up / down)	SCPC-FDMA / TDM
Transmission rate (up / down)	144 kHz / 18.577 MHz
Number of multibeam	>30
Number of channels per beam (uplink)	
102 channels (RF channels)	
- Communication channel	100
- Control channel	1
- Packet communication channel	1
Number of channels per beam (downlink)	
128 channels (slots/frame)	
- Communication channel	100
- Control channel	1
- Packet communication channel	
/ Network control, etc.	25
- Frame synchronization	2
Modulation scheme	QPSK / GMSK
User data rate	64 kb/s
Satellite TX output power	60 W
Satellite RX noise figure	3 dB
Satellite antenna diameter (up / Down)	2 m / 2.5 m

## 2.2 User Data Rate

To manufacture satellites at low cost and to make the most efficient use of the channels, it is best to unify the user data rate. A rate of 64 kb/s with 8 kHz structural integrity, which can transmit ISDN B-channel is chosen. The data rate of 64 kb/s will be one of the advantages of this system, compared with terrestrial mobile communications systems. Especially, 64 kb/s video transmission is considered to be very promising for new applications, such as portable TV phones.

The actual data rate between earth stations will be 72 kb/s, because one bit will be added to every block of 8 bits. The added bits can also be used for synchronization between the earth stations, and for detecting errors caused by "slip." The added bit pattern will be an alternating series of ones and zeros.

## 2.3 Satellite Antennas

Presently, a 2.5 m diameter antenna for transmitting and a 2 m diameter antenna for receiving are planned. These antennas have a beamwidth of about 0.2 degrees and can cover the Japanese main island with more than 30 multibeam.

## 2.4 Onboard Switching / Call Processing Capacity and User Capacity

The user capacity of the satellite can be improved through efficient demand assignment by baseband switching.

Assuming that an average number of calls per day is 4 /user, busy hour calls are 1/10 of that and that an average call duration is 1.5 minutes, the average busy hour traffic is 0.01 crl/user. Assuming the blocking probability of 0.03 and that

there are 100 channels assigned to each beam, the number of potential users per beam will be more than 9000. One satellite equipped with 3000 channels can serve more than 270,000 users.

Additionally, considering traffic condition mentioned above, the average number of busy hour calls originated in a beam is less than 1 /sec. However, considering short-time variations in the number of originated calls, the maximum number is assumed to be 5 calls/sec. Therefore the call processing capacity for all 30 beams should be more than 150 calls/sec.

## 2.5 Earth Station

Figure 2 shows how the unavailability varies according to the diameter of the earth station antenna. At present, from the viewpoint of availability it is assumed that the antenna sizes of earth stations can be classified into three types, according to the requirements of the users.

-Type 1: Availability 97-98 %. A user can use an earth station with a small aperture such as 7 x 7 cm. They offer a level of portability that cannot be provided by conventional satellite communications systems, but will not have enough margin to be used in the rain.

-Type 2: Availability 99-99.7 %. If a user needs higher availability in the rain, he can use an earth station with a larger aperture such as 30 cm diameter. Such earth stations will offer enough availability for personal use.

-Type 3: Availability 99.8-99.9 %. If a user needs an availability as high as the present Ku-band VSATs, he can use an even larger aperture earth station such as 1.2 m diameter.

The output power of type 2 and 3 earth stations should be controlled so as to minimize the interference between beams or between adjacent channels.

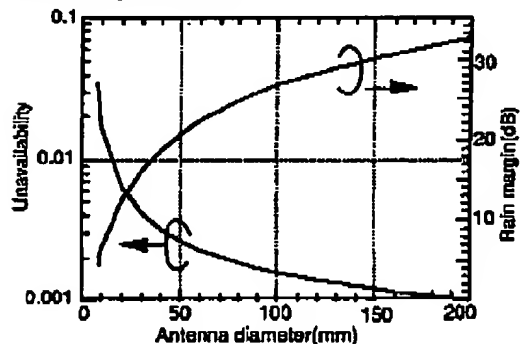


Fig. 2 Unavailability and rain margin versus antenna diameter

## 3 ONBOARD PROCESSOR

The onboard processor shown schematically in Figure 3 was designed specifically for future personal satellite communications systems. This consists of a demodulator unit and a

switch unit. A trial model of the onboard processor has already been manufactured.

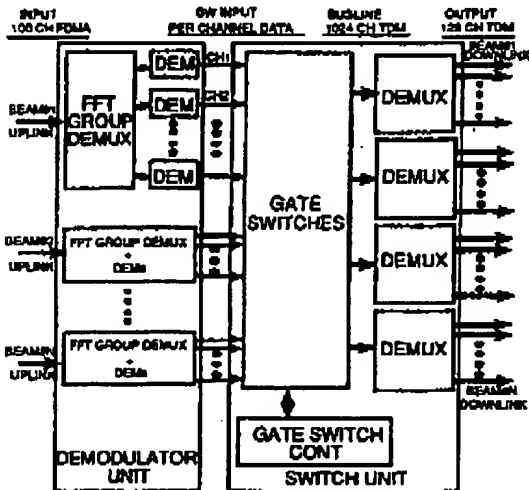


Fig. 3 Configuration of onboard processor

### 3.1 Demodulator Unit

The number of inputs to the demodulator unit is one signal per beam, or 30 lines in total. Each input is a 140 MHz intermediate frequency signal which has 102 FDM multiplexed SCPC signals internally. A total of 3060 SCPC signals from all 30 beams are demultiplexed and demodulated, and output in parallel to the switch unit as 3060 baseband signals.

We propose using digital demodulation methods so as to benefit from the power and weight reductions expected in the future through the use of ASIC technology. Some demodulation methods using digital signal processing have already been proposed [3][4][5][6][7], and a group frequency demultiplexer using FFT and a per-channel demodulator have been applied for this onboard processor[8].

Figure 4 shows a block diagram of the group demultiplexer, in which 102 FDM-multiplexed SCPC signals are demultiplexed into their respective channels, which are simultaneously converted to baseband signals with carrier frequencies close to zero. As a trial model, 16 channel group demultiplexer has been made with a sampling rate of 1.6 MHz with and a frequency spacing of 100 kHz. To realize a 100 channel group demultiplexer with a frequency spacing of 150 kHz, devices with a sampling rate of nearly 20 MHz are needed.

In per-channel demodulators, an adaptive rate-conversion (ARC) filter[4] converts the sampling rate of 100 kHz directly into a symbol rate of 64 kbaud. The algorithm for detecting clock timing errors is based on a double sampling method[4] and carrier recovery is achieved by the Costas crossover loop. Additionally, since the burst mode demodulator requires a fast

carrier acquisition, the beatless pull-in PLL is used[9].

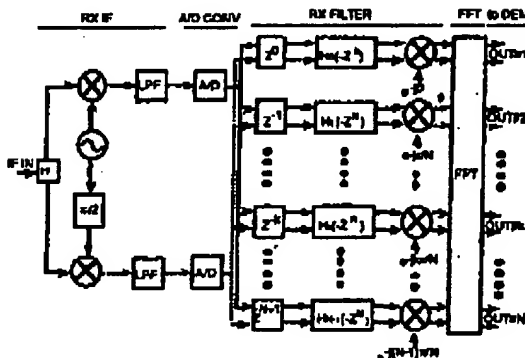


Fig. 4 Block diagram of the group frequency demultiplexer

### 3.2 Switch Unit

The switch unit consists of a circuit switch section and a switching control section. The circuit switch section carries out circuit switching based on information stored in routing pattern memories. The switching control section is mainly responsible for reception, analysis and transmission of the control data, and channel management.

SCR has developed a new switching architecture with address gates that can simultaneously synchronize, route, and multiplex a number of input signals. This architecture satisfies the functions and channel capacity required of the system in a simple configuration[8].

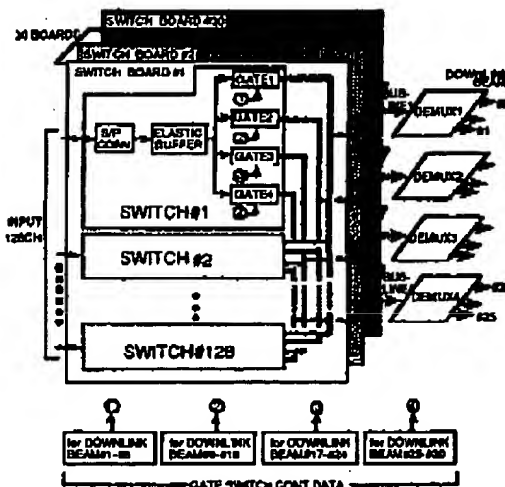


Fig. 5 Block diagram of the switch unit

A block diagram of the switch unit is shown in Figure 5.

The input serial channel data from the demodulator is converted to 9-bit parallel data, stored in an elastic buffer, and output to the buslines through the address gates. One unit of 9-bit data is the handling unit in this switch and a unique characteristic of this onboard processor. Each address gate turns on at the appointed timing according to the routing data. This gating is done in correspondence with the data rate of the busline on which more than 1000 channels are time-division multiplexed. The data on the buslines is then distributed to each downlink TDM data stream by the DEMUXs, and sent to the modulators. The data in any input channel can be routed to any time slot of any downlink TDM data stream, and can also be easily routed to two or more time slots. The latter means 1 to N connections can be available easily. Dynamic routing can be carried out by changing the data in the routing memories.

In our secondary trials, we have manufactured custom-made ASICs of a 64-input channel switch unit including S/P converters, elastic buffers, and address gates in a 24 k gate-array. Two such ASICs are equipped in a single switch board. Therefore, 30 of these switch boards can handle a switching capacity of 3000 channels.

#### 4. DEMAND ASSIGNMENT CONTROL

The onboard processor is responsible for assigning communication channel numbers by controlling the earth station directly. It is thus important to develop a demand assignment control procedure which establishes/releases connections between earth stations smoothly and makes full use of the transponder capability. It is assumed that the basic procedure is as shown in Figure 6.

The location registration procedure shown in Figure 6 is carried out when an earth station is powered on, or during an idle phase in communications when the earth station moves from one beam to another. (The beam information for location registration request is transmitted from the satellite at constant intervals of less than 1 second.) After receiving a request, the satellite registers the beam number associated with the earth station in the user ID management memory. In this way, the satellite only needs to transmit paging packets to the downlink beam associated with the destination users.

##### 4.1 Control Channel Assignment and Control Data Format

Control signals are transmitted in the exclusive FDM channel in the uplink, and exclusive TDM time slots in the downlink. These are used by all the earth stations for setting up or for releasing channels. The proposed control data format is shown in Figure 7. The control data length will be about 16 bytes. By including a preamble for carrier and clock recovery, unique word (UW) and cyclic redundancy check (CRC) bits for error detection, the total length will be about 60 bytes. The header of the data format identifies the nature of the received data. All the information required in the block, such as a destination-up channel, origination down-channel and so on, is clarified according to the set-up procedure shown in Figure 6. After the earth stations receive this information,

they can set up the communication channels and start communication. When earth stations request communication channel release, they transmit the same information with different header information.

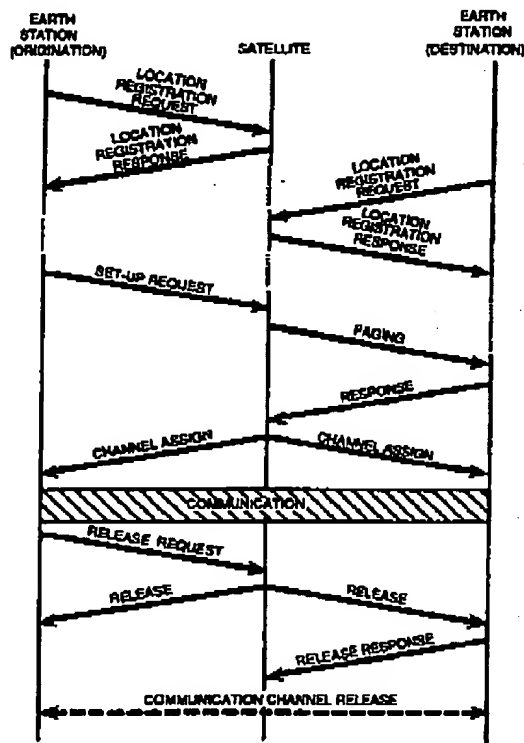


Fig. 6 Basic procedure

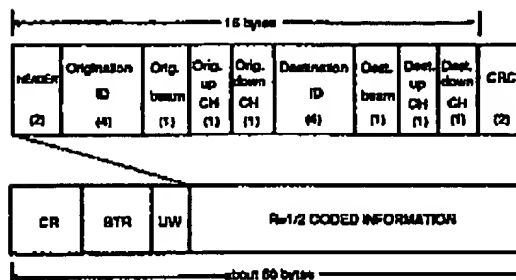


Fig. 7 Control data format

The demand assignment efficiency mainly depends on the control channel access scheme and the processor's performance. These items are described in the following sections.

#### 4.2 Control Channel Access Scheme

The transmission of the control signals to the downlink is perfectly controlled by the onboard processor. However, in the uplink, signal collisions may occur because the control signals from earth stations are transmitted randomly. Generally, pure- or slotted-Aloha schemes are effective in systems such as this, having a comparatively large number of users, but comparatively little traffic to each user.

In this system, control signals in the uplink are classified into randomly originated signals, such as set-up requests, and response signals, such as set up responses, which reply to downlink signals from the satellite such as paging signals. If either of the two schemes mentioned above is used for this system, collisions may occur randomly regardless of the signal's nature. Therefore, such schemes will have a serious effect on the connection delay time. We have thus studied a unique control channel access scheme to improve the delay time.

In this scheme, uplink control signals are transmitted in classified and pre-assigned time slots, as shown in Figure 8, assuming the maximum rate of call origination is 150 calls/sec. This assignment avoids collisions between random signals from originators, such as set-up requests and response signals from called users such as paging responses. Additionally, by controlling the transmission timing of downlink signals to called users, such as paging signals, collisions of their response signals can also be avoided. Consequently, the slotted-Aloha scheme is used only for randomly generated signals. Compared with pure- or slotted-Aloha schemes, the number of retransmissions from earth stations will be less and the connection delay performance will be improved.

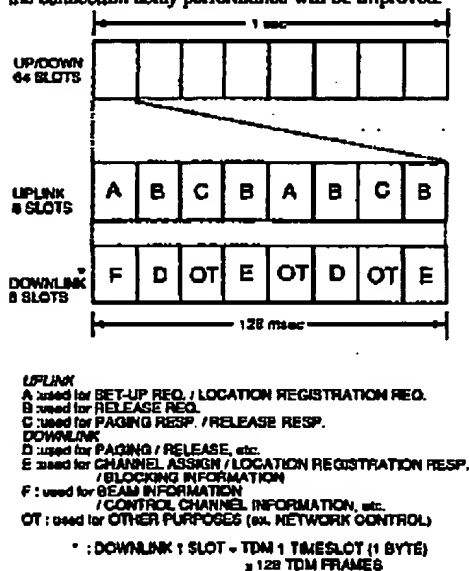


Fig. 8 Uplink/Downlink slot assignment

#### 4.3 Processor Architecture

In addition to the control channel access scheme, the quality of the control packets depend on the processor's performance. In this system, processors in the switching control section of the switch unit perform such functions as control packet reception, data analysis, formatting/transmission and switch pattern setting.

One of the most important requirements of the processor is call processing capacity. If the earth stations transmit according to the slot allocation scheme shown as Figure 8, the maximum number of control packets arriving at the satellite will exceed 1000 packets/sec. In order to process such large amount of data, a multi-processor architecture is being investigated.

Figure 9 shows the proposed processor architecture. Downlink packets formatted by processors are memorized on classified memories in the packet TX controller according to nature of packets, and these are transmitted to the switch unit according to the transmission timing shown as Figure 8. In order to allocate each received packet to the appropriate processor while keeping their load ratios almost equal, the first control packet to be received in setting up process, namely set-up requests, are distributed evenly among the processors. Subsequent packets in the same call process are allocated to the same processor so as to facilitate the process data management. A process number, which is assigned to each call, is used to perform this allocation, and is written in the header of the packet. In the processor, such processes will be made in the same manner as with a single processor, except for the channel resource management. Accordingly, it is important to find the best channel resource management.

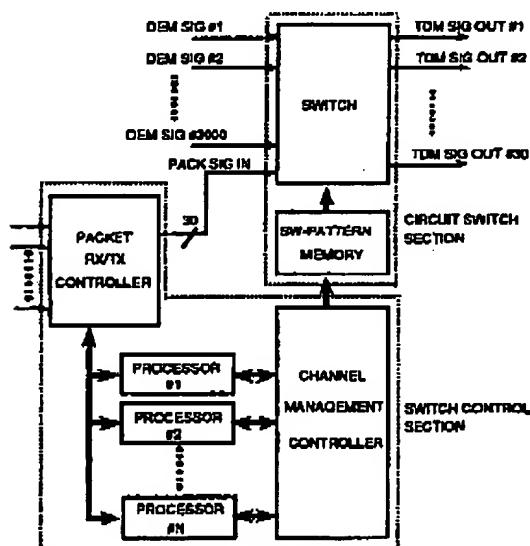


Fig. 9 Configuration of the processor architecture

#### 4.4 Channel Resource Management

Since the onboard switch has full connectivity, the channel resources to be managed are the SCPC channel number and the TDM slot number of the uplink and downlink, respectively. For a multi-processor architecture, there are two channel resource management methods involving either locally distributed memory, or centralized memory. The former requires inter-processor communications and the latter requires processor-memory communications. Due to the simplicity of its configuration and the high processor speed, the centralized memory method is preferable.

Figure 10 shows the configuration of the channel management controller, which consists of a set of channel memories and a memory control circuit. The up- or down- channel numbers allocated to each beam are stored in a corresponding memory cell (channel memory beam #i, up or down) which is used as a FIFO (first-in / first-out) memory.

The memories are first initialized with 100 channel numbers for each uplink memory and 128 channel numbers for each downlink memory. When a processor requests a channel, this section outputs a channel number which is placed at the top of the FIFO memory corresponding to the beam and its transmission direction (up or down), and sends the corresponding switch control pattern to the circuit switch section.

When the communication channels are released, channel numbers are returned from the processors to the channel management control circuit by supplying the beam number, direction and channel number. The management circuit places the returned number at the end of the corresponding FIFO and sends the switch control pattern to the switch section to close the call.

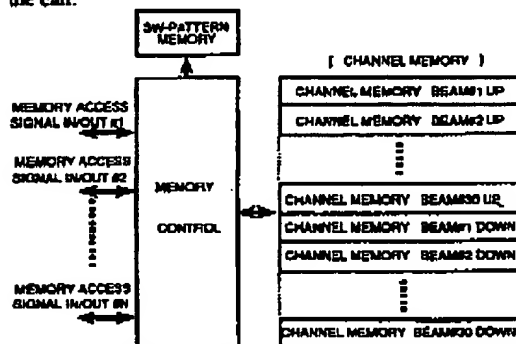


Fig. 10 Configuration of channel management controller

#### 5. SECOND TRIAL MODEL

At present, SCR is manufacturing a second trial model, mainly with a view to study the demand assignment control system. We have now finished manufacturing the switching controller, and are now developing the software for the call establishment protocol. Table 2 shows the requirements of this model, which should allow us to evaluate the design concepts

described earlier. It has an input line with 16 SCPC channels, allowing us to confirm the fundamental function and performance of the demultiplexer/demodulator. In the switch unit, a 384 x 3000 switching capability is provided, and the call establishment protocol is realized in software implemented in the design. The multi-processor architecture is included by using two micro-processors.

Table 2 Requirements of the second trial model

Input signal	140 MHz SCPC / FDMA (1 line)
Output signal	8. 257 Mb/s (30 lines)
Switching	
Method	Address gate scheme (ASIC)
Switch size	384 x 3,000 (with 4 ASICs)
Connection control	
Control/access scheme	Pre-assigned slotted-Aloha and transmission control by satellite
Call processing capacity	> 150 calls/sec
Processor configuration	
Method	Multi-processor
Number of processors	2
Channel management	
Control method	Central memory

#### 6. CONCLUSION

In this paper, the concept of a future personal satellite communications system has been proposed. This will be realized by using the onboard processor with baseband switching that SCR has been designing and developing.

The onboard switch plays an important role in this millimeter-wave personal communications system, and its performance will directly determine such feature as the switch capacity and the connection processing speed. Then, an effective architectural method for realizing such performance has been proposed.

SCR is currently developing the software for the call establishment protocol of the second trial model. Once this has been finished, we will be ready to evaluate the entire system, including the call processing performance. The technologies used in these trial models should contribute to future R&D satellite programs in Japan.

#### REFERENCES

- [1] M. Shimada, T. Iida, S. Shimoseko, Y. Ohkami, S. Kizume, and H. Kobayashi, "Missions and Technology for Advanced Communications Satellite," IAF-84-67 (1984)
- [2] I. Izumi, A. Inoue, M. Ishizu and Y. Otsu, "Research and Development of Millimeter-wave Transponder for Personal Communications," 16th ISTS. (1988)
- [3] W.H. Yim, C.C.D. Kwan, P.P. Coakley and B.G. Evans, "Multi-carrier Demodulators for On-board Processing Satellites," International Journal of Satellite

Communications, VOL.6, 243-251 (1988)

[4] F. Takahara, M. Yasunaga and Y. Hirata, "A PSK Group Modem Based on Digital Signal Processing: Algorithm, Hardware Design, Implementation and Performance," International Journal of Satellite Communications, VOL.6, 253-266 (1988)

[5] E. Del Re and R. Fantacci, "Alternatives for On-board Digital Multicarrier Demodulation," International Journal of Satellite Communications, VOL.6, 267-281 (1988)

[6] H. Gockler, "A Modular Multistage Approach to Digital FDM Demultiplexing for Mobile SCPC Satellite Communications," International Journal of Satellite Communications, VOL.6, 283-288 (1988)

[7] S. Kato, K. Ohtani, T. Kohri, M. Morikura, M. Umehira and S. Kubota, "On-board Digital Signal Processing Technologies for Present and Future SCPC Systems," International Journal of Satellite Communications, VOL.6, 289-300 (1988)

[8] M. Endo, T. Kumagai, T. Yamamoto, Y. Osu, T. Kikuchi and N. Komiyama, "Future Satellite Communications System using Millimeter-wave and Onboard Processor," ICDSC9-A1-5 (1992)

[9] J. Namiki, S. Ootani, Y. Yasuda, "QdB Eb/No Burst Mode SCPC Modem with High Coding Gain FEC," ICC'86-56.4 (1986)